Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-17 (canceled)

18. (currently amended) An isolation structure, comprising:

a first area and a second area;

a plurality of shallow isolation trenches in the first area; and

a plurality of deep isolation trenches in the second area, wherein the deep isolation trenches and the shallow isolation trenches ~~being~~ are self-aligned using a single photolithography step and at least one shallow isolation trench has a width equal to or greater than the width of at least one deep isolation trench.

19. (original) The isolation structure of claim 18, wherein the plurality of shallow trenches are between approximately 1000 Å to 2000 Å in depth.

20. (original) The isolation structure of claim 18, wherein the plurality of deep isolation trenches are between approximately 3000 Å to 6000 Å in depth.

21. (previously presented) The isolation structure of claim 18, wherein the first area includes memory devices.

22. (previously presented) The isolation structure of claim 21, wherein the memory devices comprise flash memory devices.

23. (previously presented) The isolation structure of claim 18, wherein the second area includes logic devices.

24. (currently amended) The isolation structure of claim 18, wherein the second area includes only ~~the widths of the shallow isolation trenches are less than the widths of the~~ deep isolation trenches.

25. (previously presented) The isolation structure of claim 18, further comprising:

a thin thermal oxide in the shallow isolation trenches.

26. (previously presented) The isolation structure of claim 18, further comprising:

a trench fill material in the shallow isolation trenches.

27. (previously presented) The isolation structure of claim 18, further comprising:

a first active region in the first area; and

a second active region in the second area.

28. (previously presented) The isolation structure of claim 27, further comprising:

a mask layer on the first active region.

29. (previously presented) The isolation structure of claim 28, wherein the mask layer comprises a pad oxide layer and a nitride layer.

30. (previously presented) The isolation structure of claim 29, wherein the mask layer comprises an antireflective coating.

31. (previously presented) The isolation structure of claim 18, further comprising:

a photoresist layer covering the first area, wherein the photoresist layer leaves the second area exposed.

32. (currently amended) An apparatus comprising:

a substrate having ~~self-aligned deep and~~ shallow isolation trenches in a first area and deep isolation trenches in a second area, wherein the deep and shallow isolation trenches are self-aligned using a single photolithography step; and

a photoresist layer covering the first area and leaving the second area exposed.

33. (previously presented) The apparatus of claim 32, wherein the substrate comprises monocrystalline silicon.

34. (previously presented) The apparatus of claim 32, wherein the shortest distance between a shallow isolation trench and an adjacent deep isolation trench is greater than the allowed error of a non-critical photolithography mask.

35. (previously presented) The apparatus of claim 34, wherein the allowed error is in the range of about 150 to 300 nm.

36. (currently amended) The apparatus of claim 32, further comprising:

a first active region in the first area; and

a second active region in the second area. ~~wherein the deep isolation trenches isolate active regions including high voltage logic devices.~~

37. (currently amended) The apparatus of claim 32, further comprising:

a mask layer on the first active region, wherein the mask layer comprises a pad oxide layer and a nitride layer. ~~wherein the shallow isolation trenches isolate active regions including memory devices.~~

38. (currently amended) The apparatus of claim 32, wherein the mask layer comprises an antireflective coating ~~shallow isolation trenches isolate flash memory cell columns~~.

39. (currently amended) An apparatus comprising:

a substrate including a first area and a second area;

a plurality of shallow isolation trenches in the first area;

a plurality of deep isolation trenches in the second area, wherein the deep isolation trenches and the shallow isolation trenches ~~being~~ are self-aligned using a

single photolithography step and at least one shallow isolation trench has a width equal to or greater than the width of at least one deep isolation trench;

a plurality of memory devices in the first area; and

a plurality of logic devices in the second area.

40. (previously presented) The apparatus of claim 39, wherein the memory devices comprise flash memory devices.

41. (previously presented) The apparatus of claim 40, wherein the logic devices comprise transistors to control the flash memory devices.